AMENDMENT TO THE CLAIMS

Please **CANCEL** claims 1-5, 10-12, 14-18, and 22-28.

Please **AMEND** claims 8 and 9.

This listing of claims will replace all prior versions, and listings, of claims in the application.

Claims 1-6 (Canceled).

7. (Previously Presented) A method of manufacturing a semiconductor structure, comprising the steps of:

forming a p-type field-effect-transistor (pFET) channel and a n-type field-effect-transistor (nFET) channel in a substrate;

forming a pFET stack in the pFET channel and an nFET stack in the nFET channel;

providing a first layer of material at source/drain regions associated with the pFET stack, the first layer of material having a lattice constant different than a base lattice constant of the substrate to create a compressive state within the pFET channel; and

providing a second layer of material at the source/drain regions associated with the nFET stack, the second layer of material having a lattice constant different than the base lattice constant of the substrate to create a tensile state at the nFET channel;

the first layer of material being formed by placing a mask over the nFET channel and etching the regions of the pFET and selectively growing the first layer of material within the regions of the pFET channel, and the second layer of material being formed by placing a mask over the pFET channel and etching regions of the nFET and selectively growing the second layer of material within the regions of the nFET channel;

providing a protection layer under the mask and over the nFET stack prior to the etching of the regions of the pFET stack and selectively growing the first layer of material; and

providing a protection layer under the mask and over the nFET stack prior to the etching of the regions of the pFET stack and selectively growing the second layer of material.

8. (Currently amended) ~~The method of claim 1,~~ A method of manufacturing a semiconductor structure, comprising the steps of:

forming a p-type field-effect-transistor (pFET) channel and a n-type field-effect-transistor (nFET) channel in a substrate;

forming a pFET stack in the pFET channel and an nFET stack in the nFET channel;

after the pFET stack is formed, providing a first layer of material at source/drain regions associated with the pFET stack, the first layer of material having a lattice constant different than a base lattice constant of the substrate to create a compressive state within the pFET channel; and

after the nFET stack is formed, providing a second layer of material at the source/drain regions associated with the nFET stack, the second layer of material having a lattice constant different than the base lattice constant of the substrate to create a tensile state at the nFET channel,

wherein the first layer of material is formed by placing a mask over the nFET stack, etching the regions of the pFET, and selectively growing the first layer of material within the regions of the pFET channel;

wherein the second layer of material is formed by placing a mask over the pFET stack, etching regions of the nFET, and selectively growing the second layer of material within the regions of the nFET channel; and

wherein the first layer of material and the second layer of material are each grown to a thickness about 10 to 100 nm.

9. (Currently amended) ~~The method of claim 1,~~

A method of manufacturing a semiconductor structure, comprising the steps of:

forming a p-type field-effect-transistor (pFET) channel and a n-type field-effect-transistor (nFET) channel in a substrate;

forming a pFET stack in the pFET channel and an nFET stack in the nFET channel;

after the pFET stack is formed, providing a first layer of material at source/drain regions associated with the pFET stack, the first layer of material having a lattice constant different than a base lattice constant of the substrate to create a compressive state within the pFET channel; and

after the nFET stack is formed, providing a second layer of material at the source/drain regions associated with the nFET stack, the second layer of material having a lattice constant different than the base lattice constant of the substrate to create a tensile state at the nFET channel,

wherein the first layer of material is formed by placing a mask over the nFET stack, etching the regions of the pFET, and selectively growing the first layer of material within the regions of the pFET channel;

wherein the second layer of material is formed by placing a mask over the pFET stack, etching regions of the nFET, and selectively growing the second layer of material within the regions of the nFET channel; and

wherein the first layer of material and the second layer of material are embedded in the layer.

Claims 10. -13. (Canceled).

Claims 19-28 (Canceled).